Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application. The following listing provides the amended claims with deleted material crossed out and new material underlined to show the changes made.

1-7. (Cancel).

8. (Currently Amended) ~~The IC layout of claim 1 further comprising:~~

An integrated-circuit (IC) layout comprising:

a plurality of interconnect lines;

a first set of Steiner points that are in the shape of a non-quadrilateral polygon, wherein at least two interconnect lines intersect at each Steiner point, wherein the Steiner points in the first set of Steiner points are not vias,

~~a)~~ a set of nets with routable elements; and

~~b)~~ a first set of interconnect lines for connecting the routable elements of the nets, wherein the interconnect lines have ends that are partial non-quadrilateral polygons.

9. (Original) The IC layout of claim 8, wherein the interconnect-line ends are half non-quadrilateral polygons.

10. (Original) The IC layout of claim 9, wherein the interconnect-line ends are half octagons and the Steiner points are octagons.

11. (Previously Presented) The IC layout of claim 9, wherein the interconnect-line ends are half hexagons and the Steiner points are hexagons.

12. (Cancel).

13. (Cancel).

14. (Currently Amended) An integrated-circuit (IC) layout comprising:

Cadence Docket: 2002-086 09
Attorney Docket: SPLX.P0106
PTO Serial: 10/066,102

a plurality of interconnect lines;

a first set of Steiner nodes, wherein each Steiner node in the first set has a circular shape, wherein at least two interconnect lines intersect at each Steiner node; ~~The IC layout of claim 12 further comprising:~~

~~a)~~ a set of nets with routable elements; and

~~b)~~ a first set of interconnect lines for connecting the routable elements of the nets, wherein the interconnect lines have ends that are partially circular.

15. (Original) The IC layout of claim 14, wherein the interconnect-line ends are semi-circular.

16. (Previously Presented) An integrated-circuit ("IC") layout comprising:

a) a plurality of interconnect lines, wherein the interconnect-lines have ends that are partial non-quadrilateral polygons; and

b) a plurality of Steiner points that are in the shape of a non-quadrilateral polygon, wherein at least two interconnect lines intersect at each Steiner point, wherein each of a plurality of Steiner points are not vias.

17. (Previously Presented) The IC layout of claim 16, wherein the interconnect-lines ends are half non-quadrilateral polygons.

18. (Previously Presented) The IC layout of claim 17, wherein the interconnect-line ends are half octagons and the Steiner points are octagons.

19. (Previously Presented) The IC layout of claim 17, wherein the interconnect-line ends are half hexagons and the Steiner points are hexagons.

Cadence Docket: 2002-086 09
Attorney Docket: SPLX.P0106
PTO Serial: 10/066,102